

104-248P

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)

09/380270

NEW

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		412 Recd PCT/PTO 27 AUG 1999
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	412 Recd PCT/PTO 27 AUG 1999
PCT/SE98/00347	February 26, 1998	February 28, 1997
<b>TITLE OF INVENTION</b> DATA-CONVERSION METHOD FOR MULTIBEAM LASER WRITER FOR VERY COMPLEX MICROLITHOGRAPHIC PATTERNS		
<b>APPLICANT(S) FOR DO/EO/US</b> THUREN, Anders		
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:		
1. <input checked="" type="checkbox"/>	This is a <b>FIRST</b> submission of items concerning a filing under 35 U.S.C. 371.	
2. <input type="checkbox"/>	This is a <b>SECOND</b> or <b>SUBSEQUENT</b> submission of items concerning a filing under 35 U.S.C. 371.	
3. <input checked="" type="checkbox"/>	This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).	
4. <input checked="" type="checkbox"/>	A proper Demand for International Preliminary Examination was made by the 19 <sup>th</sup> month from the earliest claimed priority date	
5. <input checked="" type="checkbox"/>	A copy of the International Application as filed (35 U.S.C. 371(c)(2)) a. <input checked="" type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau). Appln. Enclosed WO 98/38597 b. <input checked="" type="checkbox"/> has been transmitted by the International Bureau. c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US).	
6. <input type="checkbox"/>	A translation of the International Application into English (35 U.S.C. 371(c)(3)).	
7. <input checked="" type="checkbox"/>	Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)). a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau). b. <input type="checkbox"/> have been transmitted by the International Bureau. c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired. d. <input checked="" type="checkbox"/> have not been made and will not be made.	
8. <input type="checkbox"/>	A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).	
9. <input checked="" type="checkbox"/>	An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).	
10. <input type="checkbox"/>	A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).	
<b>Items 11. to 16. below concern document(s) or information included:</b>		
11. <input checked="" type="checkbox"/>	An Information Disclosure Statement under 37 CFR 1.97 and 1.98./International Search Report with cited references	
12. <input type="checkbox"/>	An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.	
13. <input checked="" type="checkbox"/>	A <b>FIRST</b> preliminary amendment. <input type="checkbox"/> A <b>SECOND</b> or <b>SUBSEQUENT</b> preliminary amendment.	
14. <input type="checkbox"/>	A substitute specification.	
15. <input type="checkbox"/>	A change of power of attorney and/or address letter.	
16. <input checked="" type="checkbox"/>	Other items or information: 1.) International Preliminary Examination Report (PCT/IPEA/409) 2.) Eight (8) Sheet(s) of Formal Drawings	

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PCT/SE98/00347

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17.  The following fees are submitted:**BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5):**

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO. .... \$970.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO ..... \$840.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO. .... \$760.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4). .... \$670.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4). .... \$96.00

**ENTER APPROPRIATE BASIC FEE AMOUNT =**

Surcharge of \$130.00 for furnishing the oath or declaration later than  20  30 months from the earliest claimed priority date (37 CFR 1.492(e)).

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510 Rec'd PCT/PTO 27 AUG 1999

104-248P

IN THE U.S. PATENT AND TRADEMARK OFFICE

APPLICANT: Anders THUREN

INT'L. APPLN. NO.: PCT/SE98/00347

SERIAL NO.: New

GROUP:

FILED: August 27, 1999

EXAMINER:

FOR: DATA-CONVERSION METHOD FOR MULTIBEAM LASER WRITER FOR VERY  
COMPLEX MICROLITHOGRAPHIC PATTERNS

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents  
and Trademarks  
BOX PATENT APPLICATION  
Washington, D.C. 20231

August 27, 1999

Sir:

The following Preliminary Amendments and Remarks are respectfully submitted in connection with the above-identified application.

IN THE SPECIFICATION:

Before line 1, insert --This application is the national phase under 35 U.S.C. §371 of PCT International Application No. PCT/SE98/00347 which has an International filing date of February 26, 1998 which designated the United States of America.--

IN THE CLAIMS:

CLAIM 3: Line 1, delete "or claim 2"

CLAIM 4: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 5: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 6: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 7: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 8: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 9: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 10: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 11: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 12: Line 1, change "any one of the preceding claims"  
to --claim 1--

CLAIM 13: Line 1, change "any one of the preceding claims"  
to --claim 1--

R E M A R K S

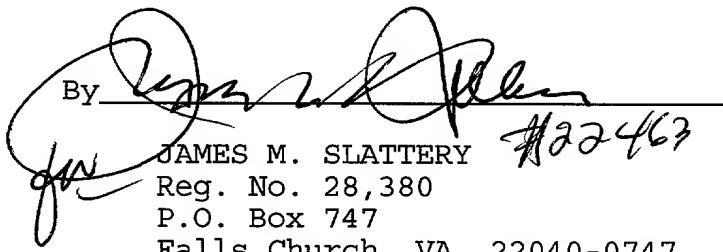
The specification has been amended to provide a cross-reference to the previously filed International Application.

The amendment(s) to the claim(s) are merely to delete the multiple dependencies and to place the application into better form prior to examination.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By   
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DATACONVERSION METHOD FOR A MULTIBEAM LASER WRITER FOR  
VERY COMPLEX MICROLITHOGRAPHIC PATTERNSField of the invention

The invention relates to microlithography, in particular to the writing of photomasks for computer displays, microelectronic devices, and precision photoetching. It is also applicable to wafers, optical devices and a variety of electronic interconnection structures such as multichip modules. Other applications are possible, such as printing and graphics, as well as laser projection displays.

Background of the invention

The application discloses a method for data conversion at extremely high through-put in a multi-beam laser plotter. The need for such high capacity comes from two sources: the ever-increasing number of features on photomasks, and increasingly sophisticated designs. For both computer displays, consumer TV screens and microelectronic products there is a rapid development towards at the same time larger sizes and smaller elemental cells. The development is most dramatic with semiconductor memories where a photomask could contain a billion elemental geometries or more. Furthermore, the elemental geometries need not be rectangular, but could be of any shape.

The input data file may be in a compacted hierarchical format, but during processing the data volume increases immensely (up to 1000-10 000 Gb per mask) and it is impossible to process the data beforehand and store the data until the time of writing. The datapath must therefore have enough processing capacity to convert the data in real time.

Another issue is the necessity of a small address grid. The writing system for semiconductor masks must be capable of writing features specified in units of 10 nm (nanometers) or less. It has been disclosed in European

(nanometers) or less. It has been disclosed in European Patent EP 0 467 076 by the same inventor that a combination of time delays and analog power modulation can be used to achieve an arbitrarily small address grid. The 5 same patent also discloses the use of several beams and parallel data paths to increase the through-put of the writing system.

For a writer with two laser beams two parallel data paths may be feasible, but current multibeam writers may 10 use up to 32 beams and simple multiplication of a single-beam datapath would be practically impossible.

There is also a strong desire to have unequal numbers of processors and beams, in particular a much larger number of processors than beams. A second need is to make the system easily scaleable, so that writers for different applications with different requirements on capacity can be configured from standard modules and running identical software.

In United States Patent US 5 533 170 a high-through-20 put multibeam data path based on parallel rasterizers is disclosed. Each rasterizer, "geometry engine", converts a frame of the pattern to a pixel map where each pixel has a greyscale value from 0 to 16. The bitmaps are distributed to beam boards via a bus system and loaded into a 25 buffer RAM area in each bus board.

The method in US 5 533 170 requires very high processing power. In particular every pixel has to be filled with its proper value and transmitted to the beam boards for writing. This is done by signal processors and custom 30 ASICs. The writing system has a burst pixel rate of 1600 million pixels per second, and extremely high demands are placed on the internal data paths. Therefore a system with parallel buses is used and the result is a complex, costly and inflexible system.

35 The present invention devices a method for data conversion that can be used on configurations from one

beam/one processor to tens of beams/hundreds of processors.

Brief summary of the invention

5 In the present invention the data conversion is divided in two steps: first cutting the geometries in scan lines and simplifying them, and then finishing the conversion of the scan lines at the point of demand, i.e. in a beam processor in the driving electronics for each  
10 beam. The idea is to make as much as possible of the conversion at the latest possible point, i.e. at the beams. What is needed at an earlier stage is to separate the data for different beams and distribute them, and to simplify the data enough to make sure that the beam processors can always handle the data flow.  
15

There are benefits with the invention in three areas:

- there is nowhere in the system a pixel map that has to be filled, therefore a lot of processing power is saved
- keeping the information to the beam processors in geometrical form instead of as a pixel map gives a smaller data volume, making the implementation simpler and more flexible. Practical tests indicate savings of 4 - 20 times depending on the pattern.
- 25 - the manipulation of the geometrical data without filling operations is well suited for algorithmic programs running on a general-purpose processor, while the final processing in the beam boards is better served with custom-logic. Using general purpose processors gives great
- 30 flexibility. It is possible to increase the performance simply by moving to faster processors as they become available, and it is easy to modify or refine the algorithms to follow the needs of the applications. Custom algorithms for specific applications or new input
- 35 formats are easily implemented.

Brief description of the drawings

Figure 1a shows how a round shape 101 combined with a triangular shape 102 are represented by a pixel map 103 with analog intensities (shown as varying shading). The beam 104 is scanning parallel lines 105. The size of the writing light spot is larger than a pixel, therefore the result on the plate will be smoothed to a round figure.

Figure 1b shows the same shapes as in Figure 1a, but where the geometrical shape are cut into segments 106 belonging to different scanlines.

Figure 1c shows the same shapes as in Figure 1b, but where the segments are replaced by a simplified new segment 107, with only length and width. As in Figure 1a the size of the spot will make the written figure smooth.

Figure 1d shows the segments in Figure 1c converted to analog values by the beam processor.

Figure 2 shows three beams 201, 202, 203 forming interlaced scan lines with the spacing 206. The figure shows that the beams scan three lines and then retrace while the stage is advanced a distance 207 equal to three times the scan spacing. There are several possible spacings 205 between the beams, here two times the scan spacing 205 is shown.

Figure 3 shows a preferred embodiment of the invention with two beams and two segmentizers.

Figure 4 shows a preferred embodiment with tree beams and four segmentizers.

Figure 5 shows how data is buffered to allow all components to run continuously at full capacity in another preferred embodiment with four segementisers and three beams.

Function of the invention

Figure 3 shows an embodiment with two processors and two beams writing on a workpiece 301 using a demagnification and focusing lens 305. The scanning and advancement between the scans, not shown in this figure, can be

done by the stage or the beams or by a combination of the two. The pattern, shown as a figure 306 in a square window 307, is described in the input data read from tape 308 or from a network 309. The input can be stored on  
5 local mass storage 310, e.g. on a local hard disk, by the host computer 311. The host computer sends the input data to the segmentizers 312, 313 after having performed any necessary format conversions, scalings, expansion of hierachical structures, etc. It may use mass storage 310  
10 for intermediate storage at any time. Furthermore it cuts the data into fields that are suitable to the length of the scan lines and to the size of the data buffers in the data path. Depending on the complexity of the data a field can be chosen to be a full writing swath or part of  
15 a swath.

The host computer sends the data for each field to one of the segmentizers 312, 313, typically in the order they need to be written and to the first available segmentizer. The host computer maintains a table of where  
20 the data for each field is and its status.

The segmentizers cut the data to each scan line and forms a list of geometrical elements for each scan line and a list of scan lines 316, 317. Although the function of the invention does not depend on it, the segmentizer  
25 may simplify the geometries in each scan line, remove any overlapping geometries and form segments that are rectangles with length and width and sort both the lists of segments and the list of scan lines in order of use by the writing hardware.

30 The list of scan lines are sent to the interlace resolvers 314, 315 where the scan lines are separated depending on which beam they will be written by. New interlaced lists for each beam are assembled. In Figure 3 the list 317 is split into the interlace lists 318 and  
35 319 that are sent to beam processor units, e.g. beam processor boards 320, 321, each with a beam processor 322 and a modulator 323. In the beam processor boards the

simplified geometry in the scan lists is resolved and converted to amplitude and time modulation of the laser beams. Since the beams are scanning the workpiece in parallel the interlaced patterns 324, 325 are reassembled  
5 in the exposed pattern.

Since only one field is written at a time only one interlace resolver can send data to the beam processors at a time as is shown by the heavy lines from 315 to 320, 321, unless the transfers are buffered so that the processing in the beam processors is decoupled from the datainput.  
10

For a simple case with a small number of beams the distribution can be done by a multiplexor, i.e. a logic circuit that accepts a single input data stream from the  
15 segmentizer/segmentizers and directs data items to different outputs according to either their position in their stream or a tag in the data item.

Figure 3 shows the method in schematic form and in a practical implementation details may vary, e.g. the two modulators can be a single physical device with two channels, each segmentizer can use one or several processors etc.  
20

#### Preferred embodiments

A preferred embodiment of the invention is in a three-beam laser writer for semiconductor reticles, as is shown in Figure 4. The writer has a distance between the scan lines of 0.25  $\mu\text{m}$  and a shortest segment length of 0.25  $\mu\text{m}$ . The maximum conversion burst rate in the beam  
25 processors is 60 million segments per second and the system is writing approximately 60 % of the total time. Accordingly the system writes  $3 * 0.25 \mu\text{m} * 0.25 \mu\text{m} * 60\%$   
30  $* 60 \text{ million} = 6.75 \text{ sq.mm/s.}$

The data distribution network must be dimensioned for the worst possible case, i.e. the entire area filled  
35 with segments of minimum length, or else it is possible to supply an input data file that causes the system to

malfunction due to data overload.. Each beam processor has a maximum burst rate of 60 million segments per second and each segment is described by two data bytes. The three beam processors therefore have a maximum data consumption of 360 Mb/s, corresponding to 180-240 Mb/s maximum sustained average rate.

The links between the interlace resolvers and the beam processors are implemented as a cross-switch network of parallel links. Each link has a transfer rate of 180 Mb/s and the shown network can at any time support three simultaneous transfers. The throughput of the links between the segmentizers and the beam processors is  $3 \times 180 \text{ mb/s} = 540 \text{ Mb/s}$  burst rate which is more than adequate for the worst possible pattern including overhead. Alternatively a simpler network can be used supporting two or only one transfer.

Figure 5 shows how generous buffers allow all components to work independent of all others. The heavy lines show current data transfers. The interlace resolvers (IR1-IR4) have two output buffers, one for storing new lists being worked on and one for storing the previous list waiting for transfer to the beam processors. Since the segmentizers are typically slower than the interlace resolvers the buffer memory between S and IR need not store any data, it needs only be large enough to allow S and IR to work in an asynchronous mode.

The beam processor units have FIFO buffers with room for several fields. Field n (Fn) is being written and is read from all FIFOs simultaneously, Fn+1 is transferred from IR1, while IR1 is working on Fn+5. IR2 and IR3 are one and two fields ahead of IR1, respectively, and the FIFOs of BP2 and BP3 are storing enough data to make the bottom of all FIFOs synchronized.

S4 and IR4 have just finished Fn+4 and IR4 is transferring the output from the work buffer to transfer buffer. At the same time the host computer HC is loading input data for a new field to S4. In actual operation the

scheduling and transfer of data is more irregular than Figure 5 leads one to believe, since the fields take different amounts of time to process and the scheduling is based on demand and availability. The buffer memories 5 in Figure 5 need not be physically separate but may be different areas in the same physical memory, and they may be reassigned dynamically. The processors P1 to P8 may likewise be 8 physical processors, but they may also be another number and they may be dynamically reassigned 10 between different tasks.

Figure 5 assumes that data needs to be loaded sequentially to the beam processor buffers. Using random-access writing instead of FIFOs would allow smaller buffer areas, but at the expense of more overhead and 15 more complex management by the host computer. In the preferred embodiment FIFOs are used.

A real pattern will have a data requirement at least 4 times smaller than the maximum data rate or 45 - 67 Mb/s. A typical writing field is part of a swath 200  $\mu$ m wide and 10 mm long needing an absolute maximum of 32 million segments or 64 Mb data, in practice not more than 8 million segments or 16 Mb data or 5.3 Mb per beam. 72 Mb buffer memory in the beam processor units (24 Mb in each unit) will then store several fields as shown in 20 Figure 5. An occasional field with too much data will cause the FIFO buffer to fill up and the pipelining will be lost for a couple fields, but the system will recover gracefully. With a larger number of processors than beams the writing hardware need only wait for data transfers, 25 not for processing since the subsequent fields are already in the transfer buffers in the IRS.

The size of the fields can be changed dynamically, so that the field size is made smaller for extremely dense patterns and larger for less dense patterns.

30 Even in the case where the data to the beam processors are only rectangular non-overlapping segments, the conversion from geometrical elements to time and power in

the beam processor uses a set of rules. First the geometry is converted to the hardware-supported time and power resolution. Secondly, the linearity between the power in the beam and the position of the edge is only approximate. When the beam is only slightly larger than the distance between two scan lines, the transient function is s-shaped and on some photo-sensitive materials there is an additional sag. Therefore it is advantageous to make an empirical calibration and store the calibration curve as a lookup table. Furthermore, if the geometrical linearity of the scan line is not perfect a stored geometrical correction table is useful.

The invention and embodiments satisfy the need for a real-time data conversion system for a wide range of applications, also the most demanding. In particular there is no hard limit to the number of processors that can be used in typical embodiments, since they use cross-switch network that is more easily extendible than bus systems. Systems designed according to the invention can also evolve with the rapidly increasing requirements on capacity. Since it is suitable to be built with standard processors, standard computer boards and software in portable high-level language, it can follow the technical development which has given a tripling of speed every two years in the past.

The terms and expressions which have been employed in the foregoing specification are used therein as terms of description and not of limitation, and there is no intention in the use of such terms and expressions of excluding equivalents of the features shown and described or portions thereof, it being recognized that the scope of the invention is defined and limited only by the claims which follow.

## CLAIMS

1. A method for fast and accurate writing of very complex patterns on a light sensitive surface comprising  
5 the steps of:

providing at least two modulated focused laser beams scanning the surface in interlaced parallel scan lines;

providing for each beam a beam processor unit with data conversion logic and means for modulating said laser  
10 beam;

providing input data containing the geometries to be written on the plate in an input format, e.g. a list of polygons;

in a first conversion step fracturing the input data  
15 into writing fields, e.g. swaths;

in a second conversion step cutting the geometries in the fractured database into scan lines, and generating for each scan line a scan list containing geometries to be written in the scan line, so called segments, and performing said second conversion step in at least two parallel processors, so called segmentizers, operating simultaneously but on different writing fields;

further distributing said scan lists to the beam processor units in accordance with the interlacing of the  
25 scan lines; and

in a third conversion step converting in said beam processor units said scan lists of segments to analog power modulation sequences for said laser beams.

2. A method as in claim 1 where in the segments in  
30 the scan lists are simplified geometrical representations of those parts of the input geometries that fall in the scan line.

3. A method as in claim 1 or claim 2 where in the segments in a scan lists are non-overlapping.

35 4. A method as in any one of the preceding claims where in the segments in a scan lists are rectangles with a length and a width.

5. A method as in any one of the preceding claims where in the segments in the scan lists are sorted in the order they will be written by the scanning beam.

6. A method as in any one of the preceding claims  
5 where in the conversion in the beam processor units uses a set of conversion rules that are empirically calibrated.

7. A method as in any one of the preceding claims where in the conversion in the beam processor units uses  
10 at least one table-lookup function.

8. A method as in any one of the preceding claims where in the scan lists are distributed to the beam processor units via a cross-switch network.

9. A method as in any one of the preceding claims  
15 where in the scan lists are distributed to the beam processor units via a bus-system.

10. A method as in any one of the preceding claims where in the scan lists are distributed to the any one of  
the preceding claims beam processor units by a multi-  
20 plexer.

11. A method as in any one of the preceding claims where in the data are pipelined through the second and third conversion steps without intermediate non-volatile storage.

25 12. A method as in any one of the preceding claims where in beam boards has an input buffer with room for the scan lists for at least two writing fields.

13. A method as in any one of the preceding claims where the transfer between the segmentizers and the beam  
30 processor unit are doubel buffered, in one output buffer in the segmentizer and in one input buffer in the beam processor unit.

14. An apparatus for fast and accurate writing of very complex patterns on a light sensitive surface comprising:  
35

at least two modulated focused laser beams scanning the surface in interlaced parallel scan lines;

for each laser beam a beam processor unit with data conversion logic and means for modulating said laser beam;

means for accepting input data containing the geometries to be written on the plate in an input format, e.g. a list of polygons

data processing means for in a first conversion step fracturing the input data into writing fields, e.g. swaths;

parallel data processing means for in a second conversion step cutting the geometries in the fractured database into scan lines, and generating for each scan line a scan list containing geometries to be written in the scan line, so called segments;

15 data distribution means for distributing said scan lists to the beam processor units in accordance with the interlacing of the scan lines; and

20 data conversion and beam modulation means in the beam processors units for, in a third conversion step, converting said scan lists of segments to analog power modulation sequences on said laser beams.

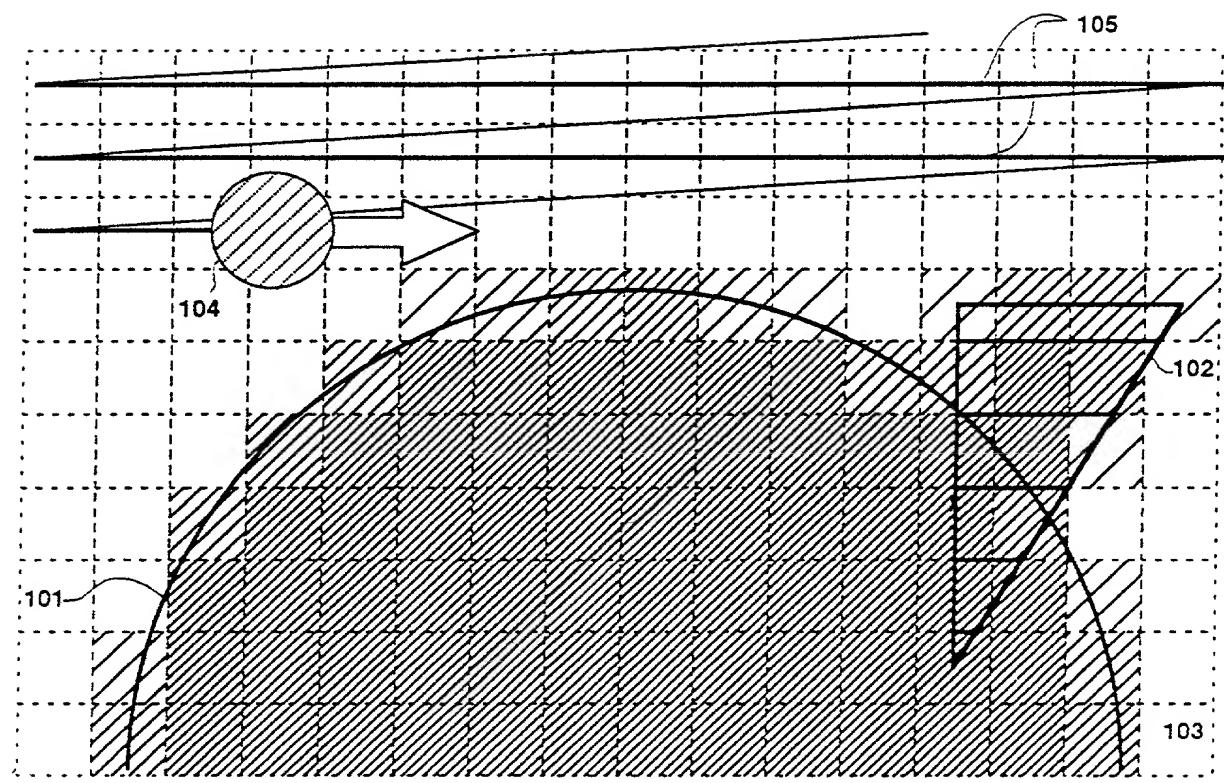


Figure 1a

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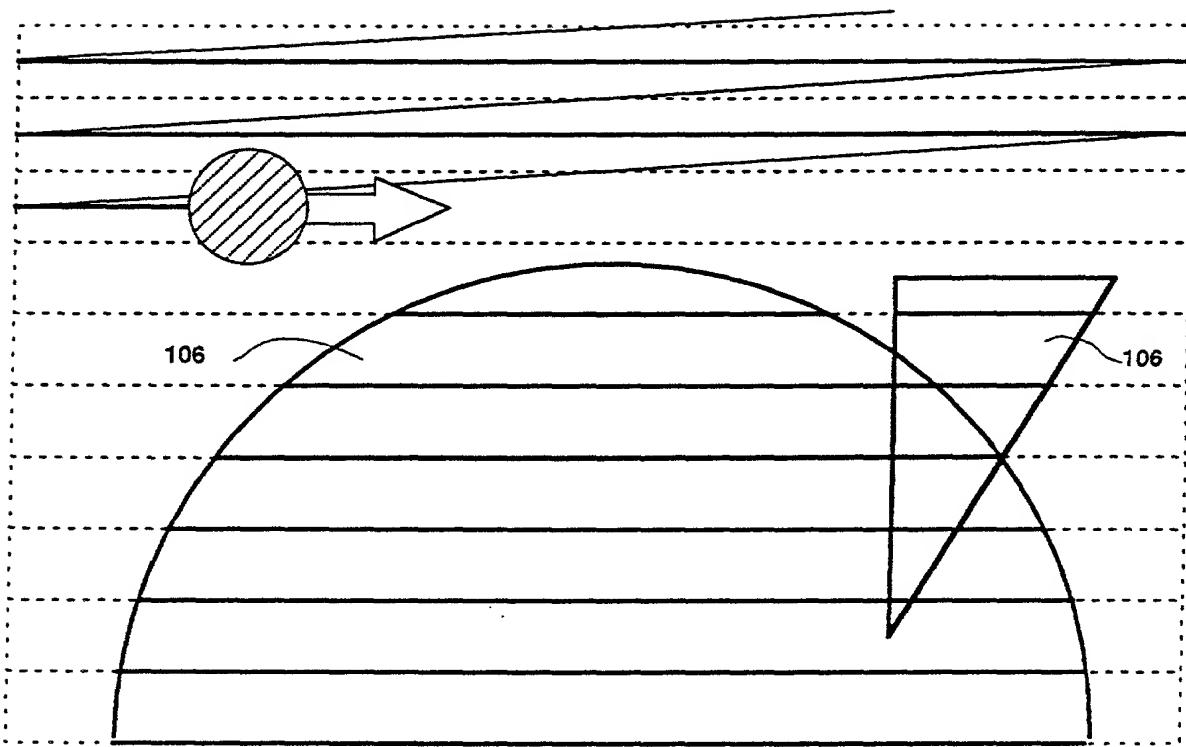


Figure 1b:

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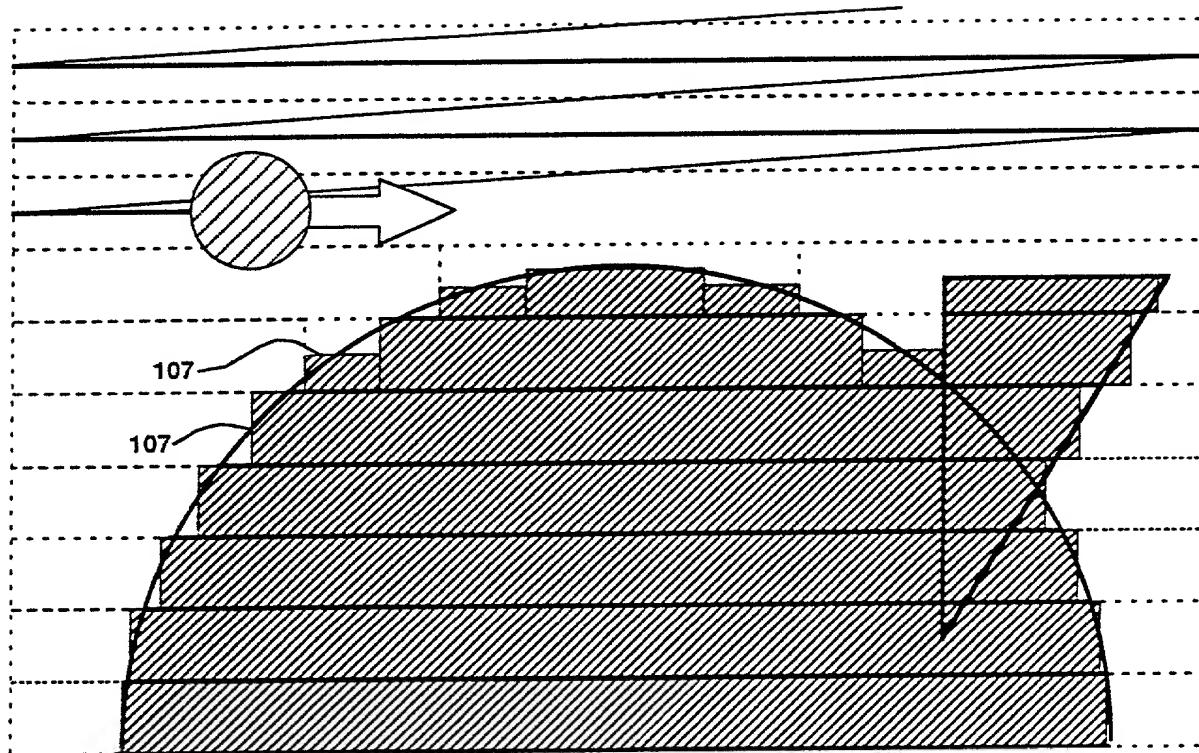


Figure 1c

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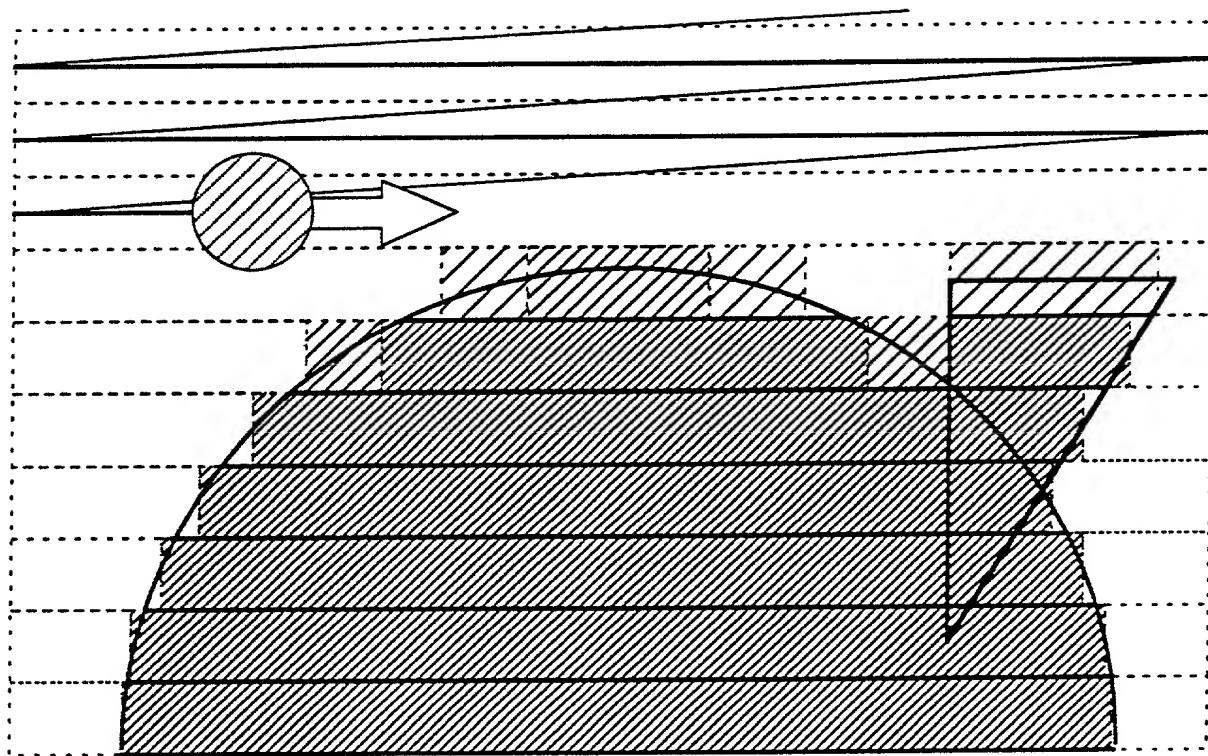


Figure 1d

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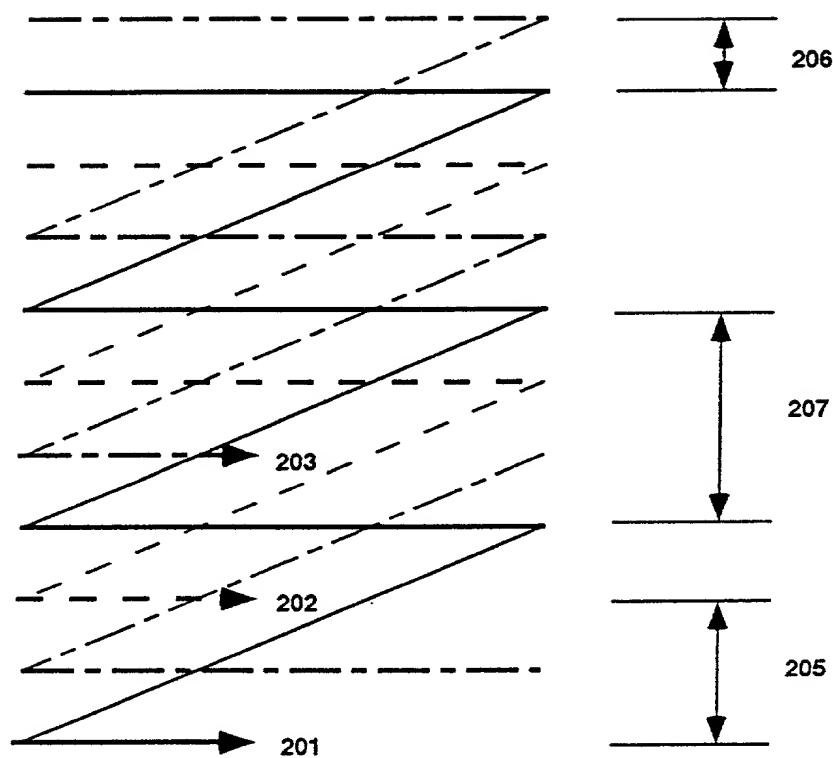


Figure 2

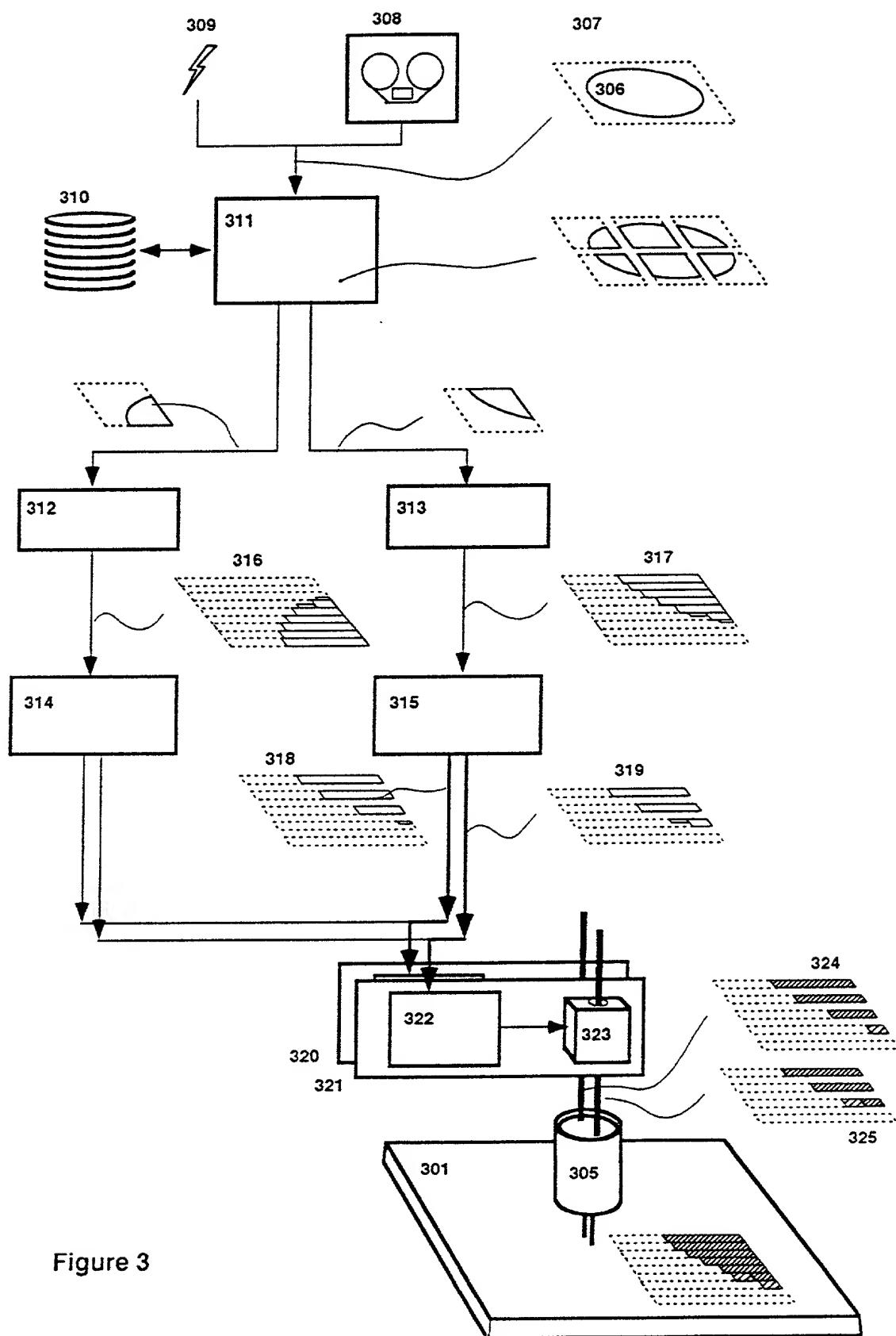


Figure 3

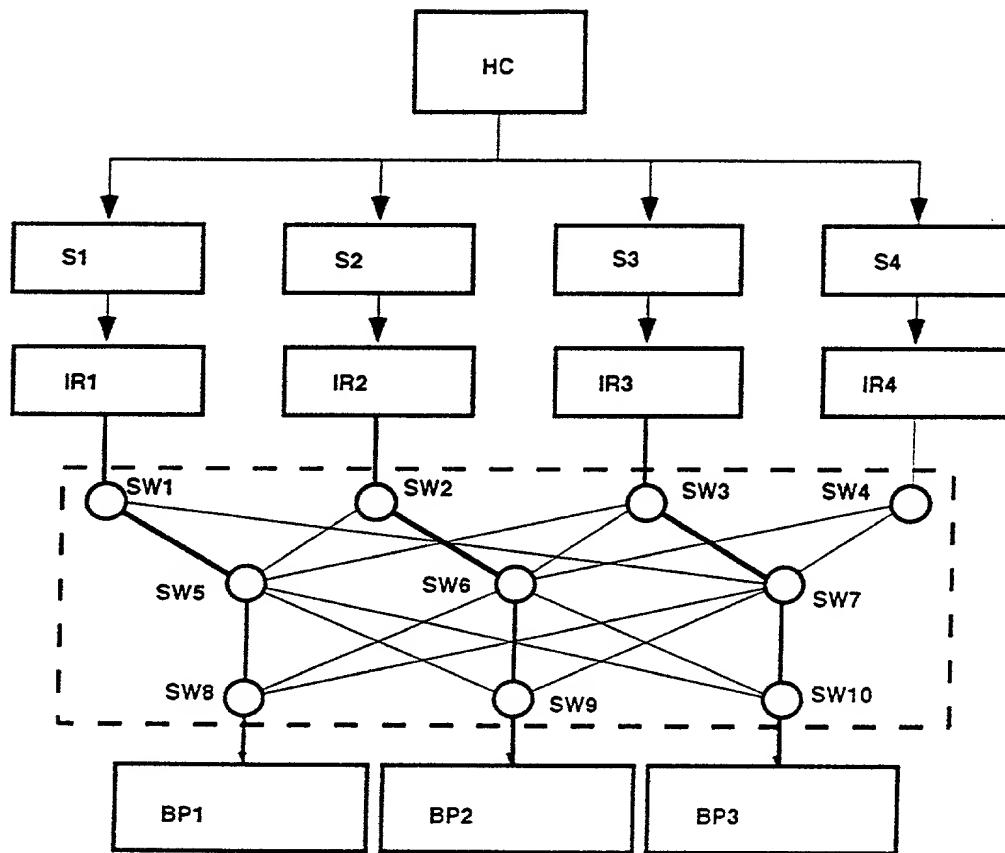


Figure 4a

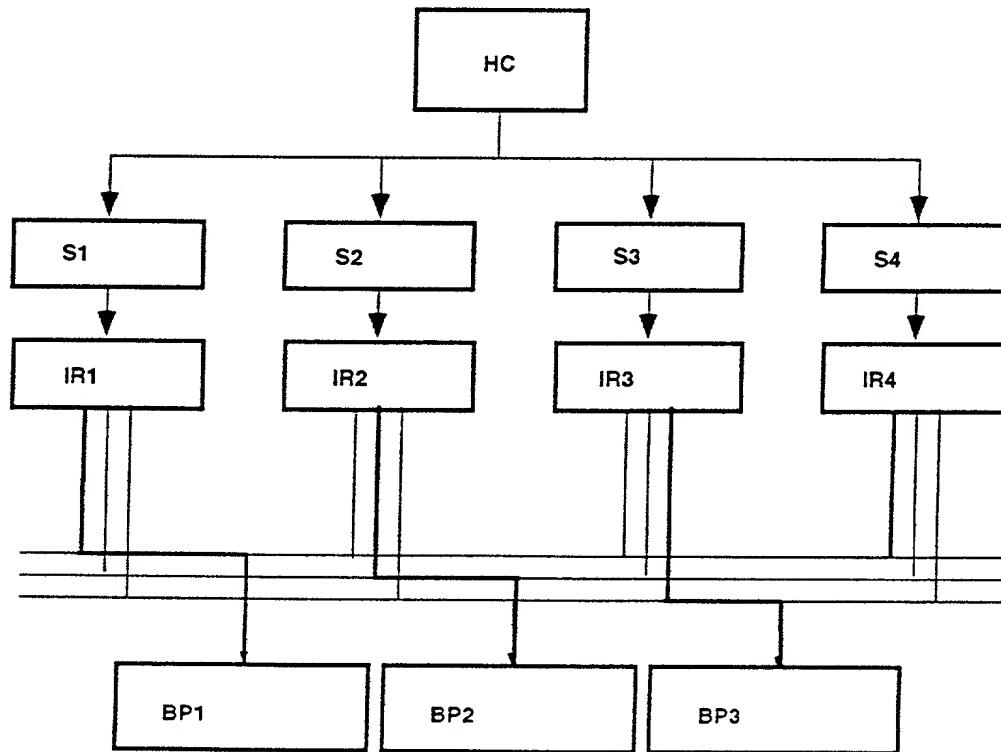


Figure 4b

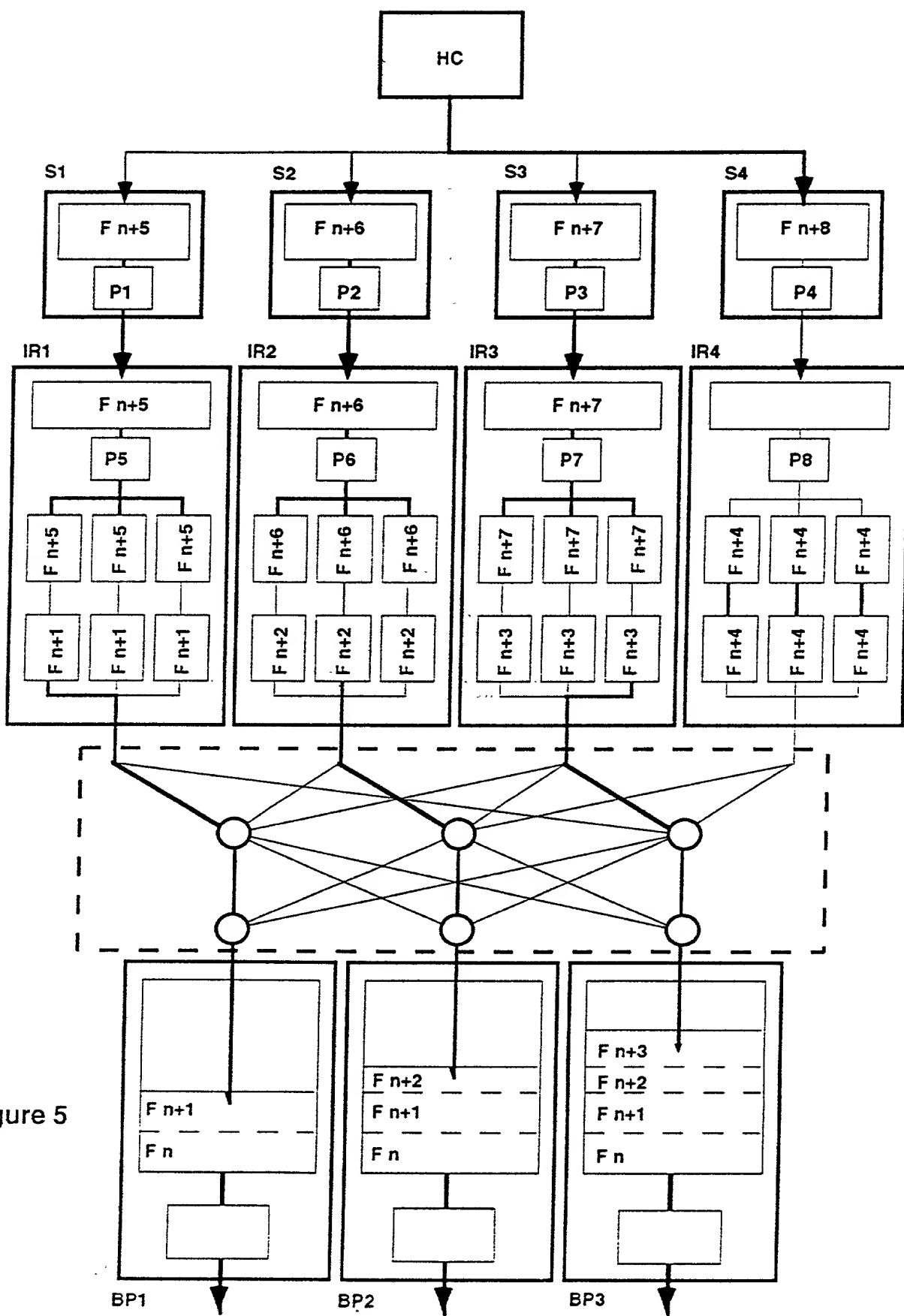


Figure 5

## BIRCH, STEWART, KOLASCH &amp; BIRCH, LLP

104-248P

PLEASE NOTE:  
YOU MUST  
COMPLETE THE  
FOLLOWING

P.O. Box 747 - Falls Church, Virginia 22040-0747  
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

**COMBINED DECLARATION AND POWER OF ATTORNEY  
FOR PATENT AND DESIGN APPLICATIONS**

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verify believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title.

DATA-CONVERSION METHOD FOR A MULTIBEAM LASER WRITER FOR VERY COMPLEX MICRO-LITHOGRAPHIC PATTERNS

Fill in Appropriate Information -  
For Use Without Specification Attached:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on \_\_\_\_\_ as  
United States Application Number \_\_\_\_\_  
and amended on \_\_\_\_\_ (if applicable) and/or  
the specification was filed on February 28, 1998 as PCT  
International Application Number PCT/SE98/00347; and was  
amended under PCT Article 19 on \_\_\_\_\_ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.  
I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

## Prior Foreign Application(s)

## Priority Claimed

9700742-1 (Number)	Sweden (Country)	February 28, 1997 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications(s) listed below.

Insert Provisional Application(s).  
(if any)

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Insert Requested Information  
(if appropriate)

Country	Application Number	Date of Filing (Month/Day/Year)
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S.  
Application(s):  
(if any)

_____ (Application Number)	_____ (Filing Date)	(Status - patented, pending, abandoned)
_____ (Application Number)	_____ (Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

Raymond C. Stewart Joseph A. Kolasch Bernard L. Sweeney Charles Gorenstein Leonard R. Svensson Andrew D. Meikle Joe McKinney Muncy Donald J. Daley John A. Castellano	(Reg. No. 21,066) (Reg. No. 22,463) (Reg. No. 24,448) (Reg. No. 29,271) (Reg. No. 30,330) (Reg. No. 32,868) (Reg. No. 32,334) (Reg. No. 34,313) (Reg. No. 35,094)	Terrell C. Birch James M. Slattery Michael K. Mutter Gerald M. Murphy, Jr. Terry L. Clark Marc S. Weiner C. Joseph Faraci John W. Bailey	(Reg. No. 19,382) (Reg. No. 28,380) (Reg. No. 29,680) (Reg. No. 28,977) (Reg. No. 32,644) (Reg. No. 32,181) (Reg. No. 32,350) (Reg. No. 32,881)
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Send Correspondence to: **BIRCH, STEWART, KOLASCH & BIRCH, LLP**  
P.O. Box 747 • Falls Church, Virginia 22040-0747  
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

PLEASE NOTE:  
 YOU MUST  
 COMPLETE  
 THE  
 FOLLOWING:  
 ↓

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code so that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

<input checked="" type="checkbox"/> Full Name of First Inventor or Sole Inventor <input type="checkbox"/> Inventor Name of <input type="checkbox"/> Invent Date This Document is Signed  <input type="checkbox"/> Invent Residence <input type="checkbox"/> Invent Citizenship  <input type="checkbox"/> Invent Post. Office Address  <input type="checkbox"/> Full Name of Second Inventor if any: <i>see above</i>  <input type="checkbox"/> Full Name of Third Inventor, if any: <i>see above</i>  <input type="checkbox"/> Full Name of Fourth Inventor, if any: <i>see above</i>  <input type="checkbox"/> Full Name of Fifth Inventor, if any: <i>see above</i>	1-00	GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
		<u>Anders</u> <u>Thurén</u>	<u>A</u> <u>S</u>	<u>99.08.25</u>
		Residence (City, State & Country) <u>Täby</u> <u>Sweden</u>		CITIZENSHIP <u>SEX</u> <u>Swedish</u>
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		GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
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		GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
		Residence (City, State & Country)		CITIZENSHIP
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		GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
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		POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
		GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
		Residence (City, State & Country)		CITIZENSHIP
		POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		

\*DATE OF SIGNATURE